NEW SCHEME

CS33

Reg. No. | | | | | | | | | | |

Third Semester B.E. Degree Examination, January/February 2006

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.) (Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. (a) Prove the following consensus laws using Boolean postulates.

i) $xy + yz + \overline{x}z = xy + \overline{x}z$

ii) $(x+y)(y+z)(\overline{x}+z) = (x+y)(\overline{x}+z)$ **(4 Marks)**

(b) Prove that if $\overline{w}x + y\overline{z} = 0$ then

$$wx + \overline{y}(\overline{w} + \overline{z}) = wx + xz + \overline{x}\,\overline{z} + \overline{w}\quad\overline{y}z$$ **(6 Marks)**

(c) Mention the different methods available for manipulating Boolean formulas. Explain any three in detail. **(10 Marks)**

2. (a) Using graphical procedure, obtain a nor-gate realization of the Boolean expression

$$f(w, x, y, z) = \overline{w}z + w\overline{z}(x + \overline{y})$$ **(6 Marks)**

(b) Show that $A \odot B \odot C \odot D = \sum m(0, 3, 5, 6, 9, 10, 12, 15)$ **(4 Marks)**

(c) Using Karnaugh maps, determine the minimal sums and minimal products for

$$f(w, x, y, z) = \sum m(0, 1, 3, 7, 8, 12) + dc(5, 10, 13, 14)$$

Is your answer unique? **(10 Marks)**

3. (a) Using the Quine-Mccluskey method and prime implicant table reductions, determine the minimal sums for the incomplete Boolean function

$$f(v, w, x, y, z) = \sum m(4, 5, 9, 11, 12, 14, 15, 27, 30) + dc(1, 17, 25, 26, 31)$$ **(10 Marks)**

(b) Explain the procedure for loading a K-map using map entered variable technique. Write the map entered variable K-map for the Boolean function.

$$f(w, x, y, z) = \sum m(2, 9, 10, 11, 13, 14, 15)$$ **(10 Marks)**

4. (a) Explain the operation of a two input TTL nand-gate with totem-pole output with a neat circuit diagram. **(8 Marks)**

(b) What is a FET? Explain how to construct a resistor with the n-channel, enhancement type MOSFET. **(6 Marks)**

(c) Explain with the help of a circuit diagram the operation of a two input CMOS nor-gate. **(6 Marks)**

5. (a) Explain a 4-bit parallel adder with carry lookahead scheme. **(10 Marks)**

(b) What is an encoder? Explain an 8-to-3 line encoder. **(4 Marks)**

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(c) Implement a full adder circuit with a 3-to-8 line decoder and two OR gates. **(6 Marks)**

6. (a) Implement the following Boolean function with an 8 x 1 multiplexer with A, B and D connected to selection lines S_2, S_1, and S_0 respectively.

$$F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$$ **(6 Marks)**

(b) Implement the following Boolean expressions using a PROM.

$$f_1(x_2, x_1, x_0) = \sum m(0, 1, 2, 5, 7)$$

$$f_2(x_2, x_1, x_0) = \sum m(1, 2, 4, 6)$$ **(6 Marks)**

(c) Explain the different types of flipflops along with their truth table. Also explain the race-around condition in a flipflop. **(8 Marks)**

7. (a) Design a synchronous mod-3 counter with the following binary sequence using clocked JK flipflops.

Count sequence : 0, 1, 2, 0, 1, 2, ... **(10 Marks)**

(b) Explain the Mealy model and Moore model of a clocked synchronous sequential network. **(10 Marks)**

8. Write short notes on :

a) Implies and subsumes

b) Fan-in and Fan-out

c) Universal shift register

d) Programmable logic arrays **(4×5=20 Marks)**

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